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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,654	09/18/2003	David Jia Chen	ROC920030233US1	8565

23334 7590 10/17/2005

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 10/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/665,654	CHEN ET AL.	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a reply to Applicant's amendment filed on 09/08/2005.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> A person shall be entitled to a patent unless –

2. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al. (U.S. Patent No. 5,602,798).

With respect to claim 1, 9 and 10, Sato et al. discloses, in Fig. 14A and col. 14, lines 35-36, a circuit arrangement comprising a) an input signal [ID1] to be delayed and b) a series of at least two delay stage [60a-60n], wherein each of the delay stages includes a stack of uniform *("same structure"; see col. 14, lines 35-36)* transistors [P3, N1] with a first group of a first conductivity type [p-channel] and a second group of transistors of a second conductivity type [n-channel] without using extended channel length transistors in the delay stages so that, *as a result*, tolerances across the delay stages track tolerance of other circuits on a chip; wherein the use of uniform channel length transistors, *as a result*, provides uniform tolerance variations and increases parametric tracking of device characteristics including delays in timing circuits across the other circuits in the chip; wherein a gate of each of the transistors in each of the delay stages are electrically coupled together to form an input in each of the delay stages, wherein a source of a top transistor in the stack is coupled to a first reference voltage [Vcc], wherein a source of a bottom transistor in the stack is coupled to a second reference voltage [ground], and wherein a

drain of the top transistor is electrically coupled to a drain of the bottom transistor in the stage so as to form an output of the stage; wherein when the input signal to be delayed is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive; and wherein when the input signal to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

With respect to claim 2, Sato et al. discloses, in Fig. 14A, that each stack of transistors includes additional transistors electrically coupled with the top transistor [P3] and the bottom transistor [N1]; wherein a drain of a first additional transistor [P2] is electrically coupled to a source of the top transistor, a drain of the last additional transistor [N2] is connected to a source of the bottom transistor, and wherein a drain of each of zero or more remaining additional transistors is electrically coupled to a source of an adjacent transistor within the remaining additional transistors so as to form a totem pole configuration for the stack.

With respect to claims 3-6, Sato et al. discloses, in Fig. 14A, that delay elements comprised both n-channel FET and p-channel FET.

With respect to claims 7 and 8, Sato et al. discloses, in Fig. 14A, that the input signal to be delayed is a clock signal.

With respect to claim 11, Sato et al. discloses, in Fig. 14A and col. 14, lines 35-36, a delay circuit comprising at least one stack of transistors, each of the at least one stack of transistors comprising a first transistor [P3] with a source electrically coupled to a first reference voltage [Vcc]; a last transistor [N1] with a source electrically coupled to a second reference voltage [Ground]; a totem pole of at least two transistors, the totem pole including: a top

transistor [P2] with a source electrically coupled to a drain of the first transistor; a bottom transistor [N2] with a source electrically coupled to a drain of the last transistor and at least two transistors, wherein the transistors complete the totem pole arrangement, wherein a drain of each of the transistors is electrically coupled to a source of an adjacent transistor within the transistors relative to the each of the transistors, and wherein each of the transistors within the totem pole comprise a uniform *("same structure"; see col. 14, lines 35-36)* channel length transistor with a first group of transistors of a first conductivity type and a second group of transistors of a second conductivity type without using extended channel length transistors in the delay stages so that, *as a result*, tolerances across the delay stages track tolerate of other delay circuits on a chip, the use of uniform channel length transistors, *as a result*, provides uniform tolerance variations and increase parametric tracking of device characteristics including delays in timing circuits across the other delay circuits; an input electrically coupled to each gate within the totem pole; and an output electrically coupled to connection between one source and one drain of two transistors within the totem pole; wherein when the input is in a low state, each transistor of the first conductivity type is active and each transistor of the second conductivity type is inactive: and wherein when the input to be delayed is in a high state, each transistor of the first conductivity type is inactive and each transistor of the second conductivity type is active.

With respect to claims 12-14, Sato et al. discloses, in Fig. 14A, that delay elements comprised both n-channel FET and p-channel FET.

Remarks and Conclusion

3. Applicants' arguments with respect to claims 1 and 9-11 filed on 09/05/2005 have been seriously considered but are moot in view of the new ground(s) of rejection due to Applicant's amendment to the claims.

4. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Fri, Monday - Thursday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER